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InES Institute of Embedded Systems

Avoiding pitfalls in PROFINET RT and IRT Node Implementation

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PI UK Conference 23/24 June 2015

Our claim to fame

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InES Institute of Embedded Systems

- InES has expertise in industrial communication technology
  - Institute of the School of Engineering, Zurich University of Applied Sciences
  - Applied R&D institute, founded in 2002
  - Focused on industrial communication, wired and wireless
  - Employs between 30-40 full time researchers
  - Financed through governement sponsered research and direct industry contracts
- Real Time Ethernet Research Group
  - 6-12 full time researchers
  - Founding member of the EPSG
  - First international PROFINET Competence Centre

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Our claim to fame

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- Real Time Ethernet Research Group
  - 6-12 full time researchers
  - Founding member of the EPSG
  - First international PROFINET Competence Centre
  - Increasing Functional Safety and Dependability expertise
  - Sideline in autonomous robotics
    - Ffi. Safe vision for autonomous robots
    - Industry 4.0 -> piece guided robot arms

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easyIRT

- InES produced the industrial proof-of-concept for the fast variant of PROFINET IRT
- This resulted in easyIRT, a VHDL communication controller for IRT and RT
- The IP has been implemented on FPGA's from Altera, Actel and Xilinx.
- Licensed in partnership with Enclustra

ENCLUSTRA
FPGA SOLUTIONS

- Close cooperation with

XILINX
ALL PROGRAMMABLE™

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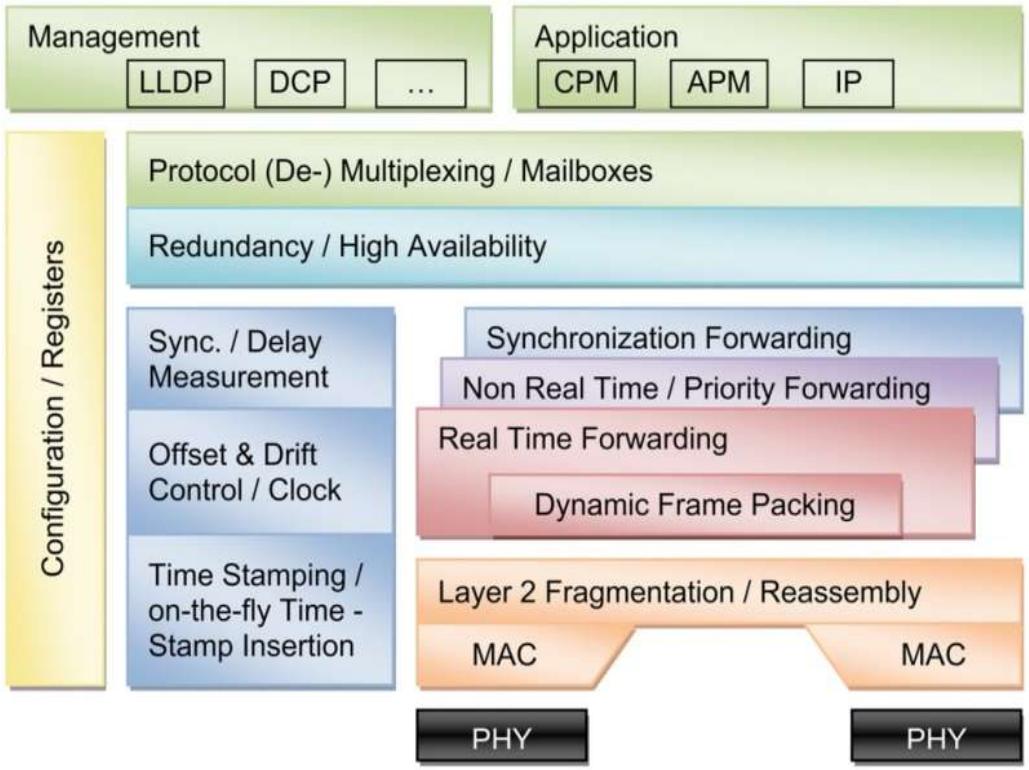
easyIRT

- easyIRT graduated from proof-of-concept for sub 250 us PROFINET to «standard» IRT down to PROFINET RT
- Much work recently done on PROFINET RT



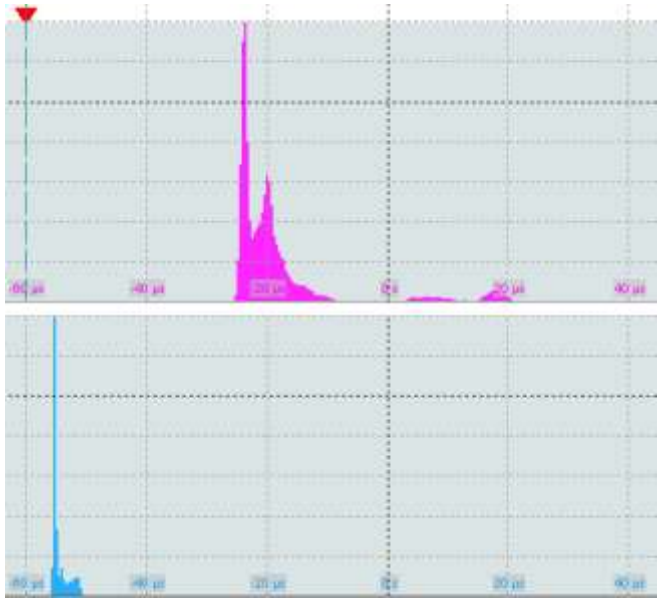
Important Question

- Can I implement PROFINET on a standard microcontroller?
  - maybe, maybe not

- Largely the last 10 years has been spent discovering what can be achieved with how much effort
- … apart from actually implementing the protocols

RT or IRT or IRT+

- Two main parts of PROFINET
  - PROFINET RT
    - Cycle times down to ~1 ms unsynchronised
  - PROFINET IRT
    - Cycle times <= 250 us, > 250 us, synchronisation precision 1 us
      - Difficult to achieve with a microcontroller



100MHz. NIOS II running eCOS

- (POWERLINK)
  - 75Mhz. ARM @1 ms cycle time
  - -> Required SoC frame transmission every 1ms
  - Interrupt at ca. 950 us and polled for timer == 1ms
  - +- 500 ns jitter
  - Dedicated layer 2 processor

PROFINET RT on a uC?
Issue Nr 1

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- Size of Stack
  - Siemens (source code)
    - Supports all features
    - > 1 Mbyte binaries
    - Low(er) licensing costs
  - Molex (Source Code)
    - Supports only 1 AR
    - ~500 kByte binary
- 1 ms is the critical cycle time

- In Contrast: EtherNet/IP
  - Molex Stack (source code)
    - 75 MHz ColdFire
    - 32 kB SRAM
    - 256 MB FLASH
    - uTasker OS
    - 2 ms cycle time

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PROFINET RT on a uC?
Issue Nr 2

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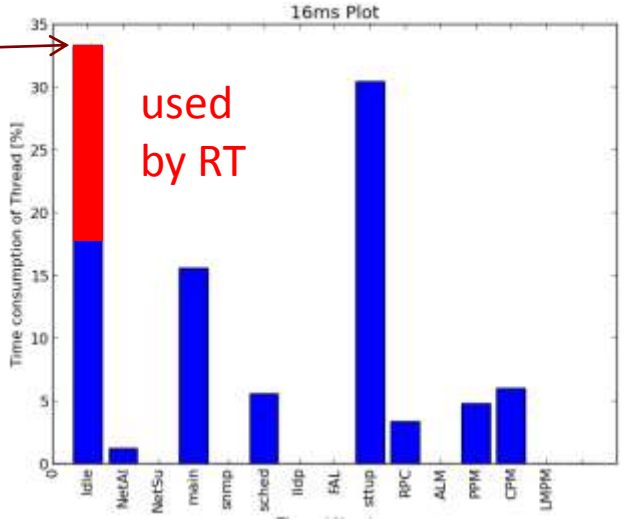
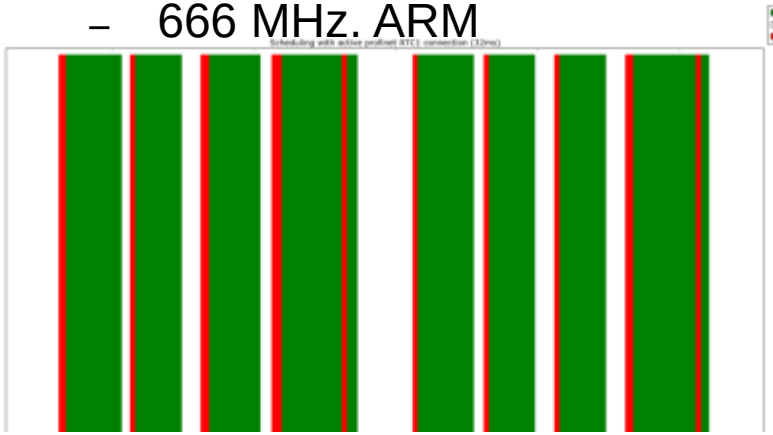
- Processor Load
  - Cyclone IV SoC
  - 666 MHz. ARM

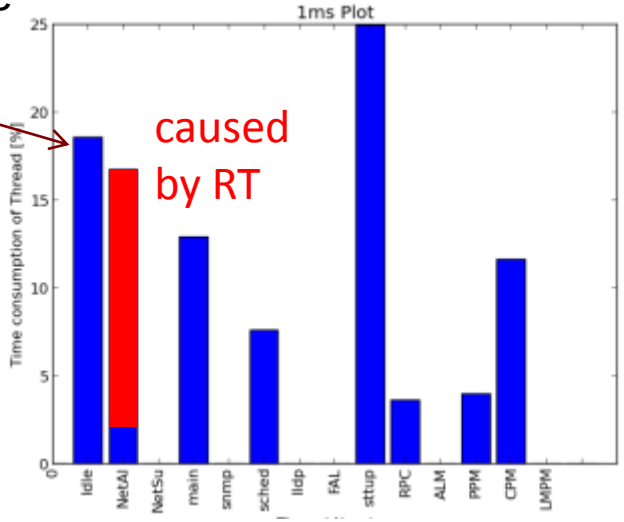
@16 ms cycle time 34% idle



@32 ms cycle time



@1 ms cycle time 18% idle



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PROFINET RT on a uC?
Issue Nr 3

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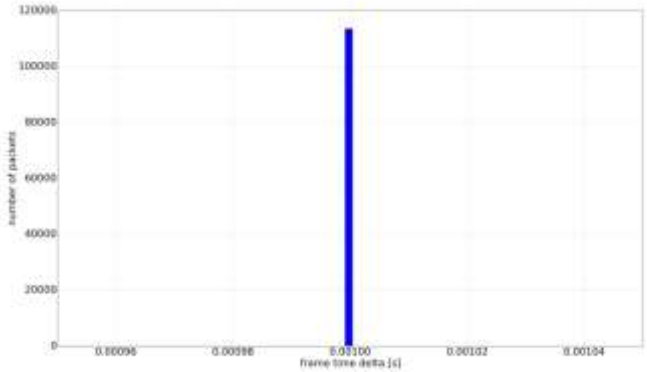
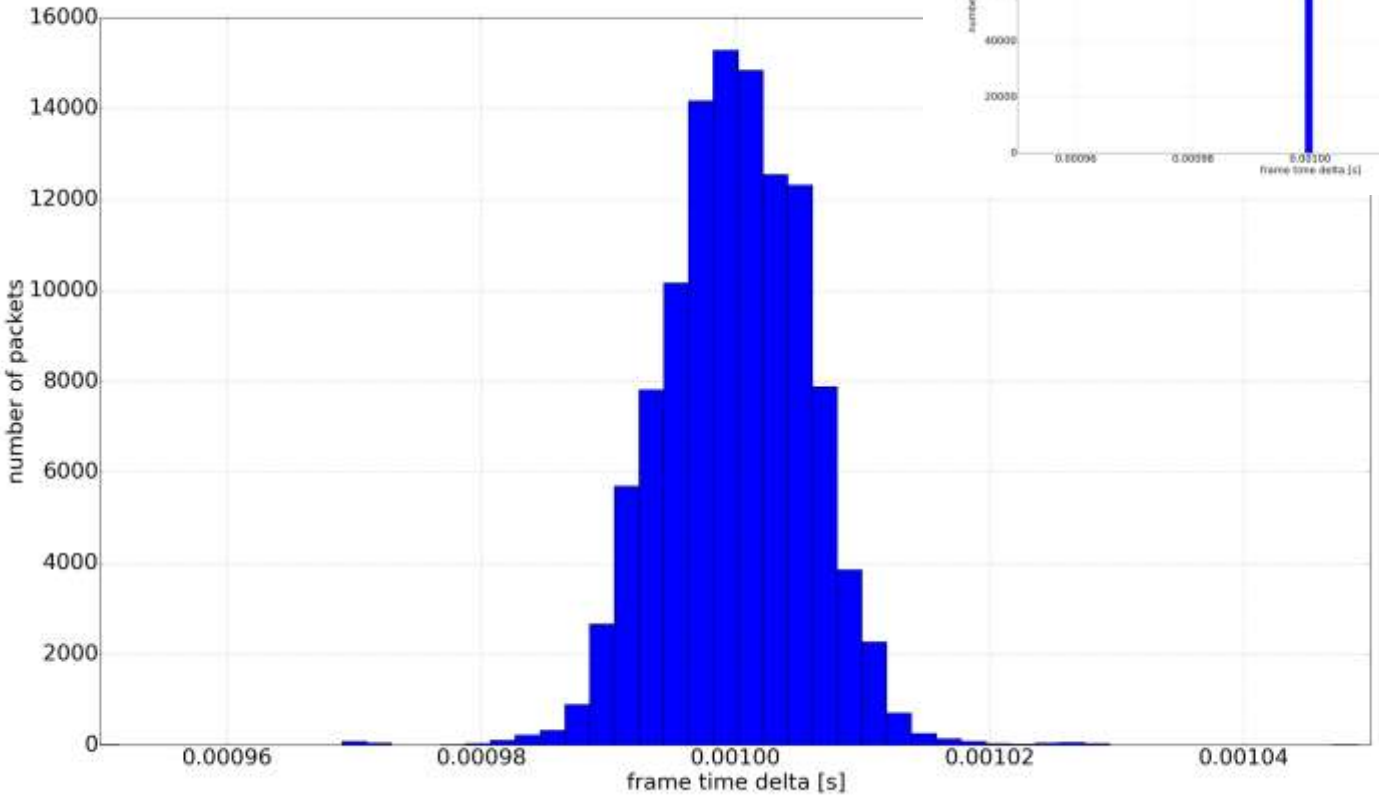
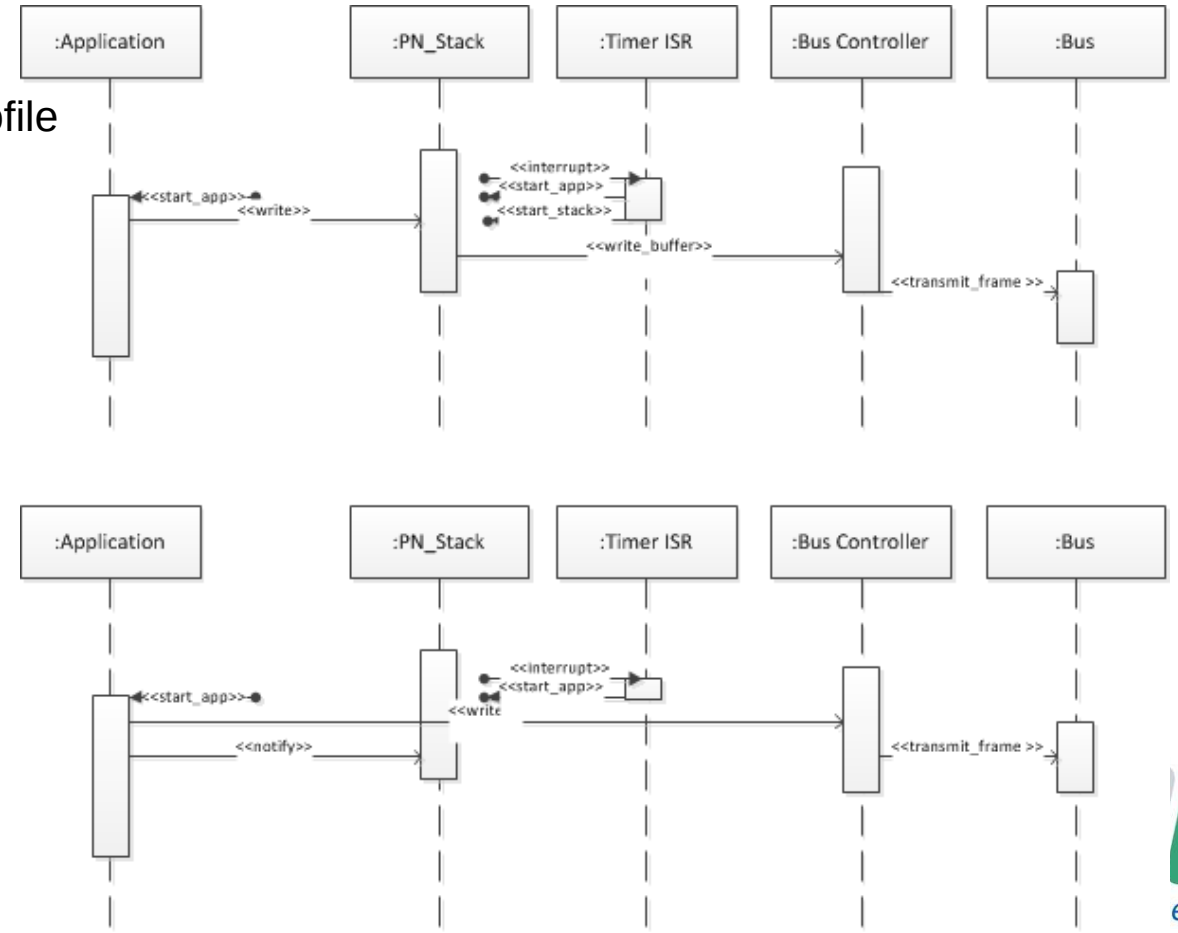
- Timing Capabilities
  - Cyclone II NIOS II @ 100MHz.





PROFINET RT on a uC?
Ramifications Issues Nr 2 & 3

- Nr 1: Hardware Acceleration
  - Reduce the SW load for routine I/O Tx/Rx
  - Cycle times < 1ms
  - Tightening of Tx profile



PROFINET RT on a uC?
Ramifications Issues Nr 2 & 3

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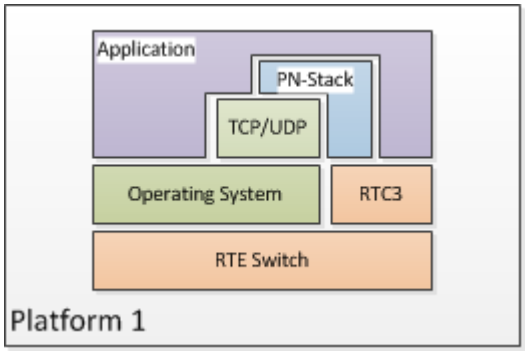
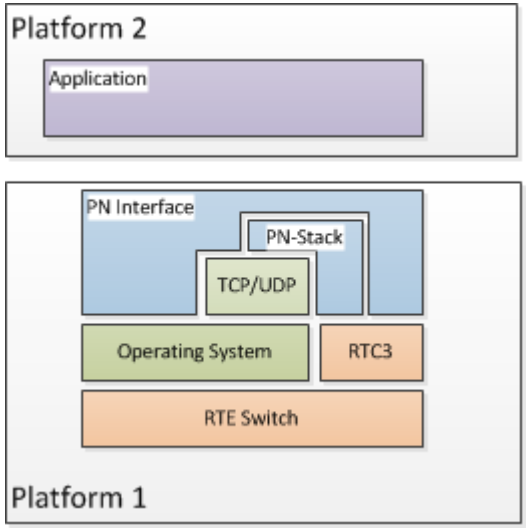
- Nr 2: Business Case for Communication Module, ASIC and Intellectual Property (IP) solutions.



ASIC / Programmable Fabric

- ERTEC
- NetX
- Tiger
- Sitara
- easyIRT
- Device Firmware RT/IRT



ASIC / Module / Programmable Fabric

- anybus
- unigate

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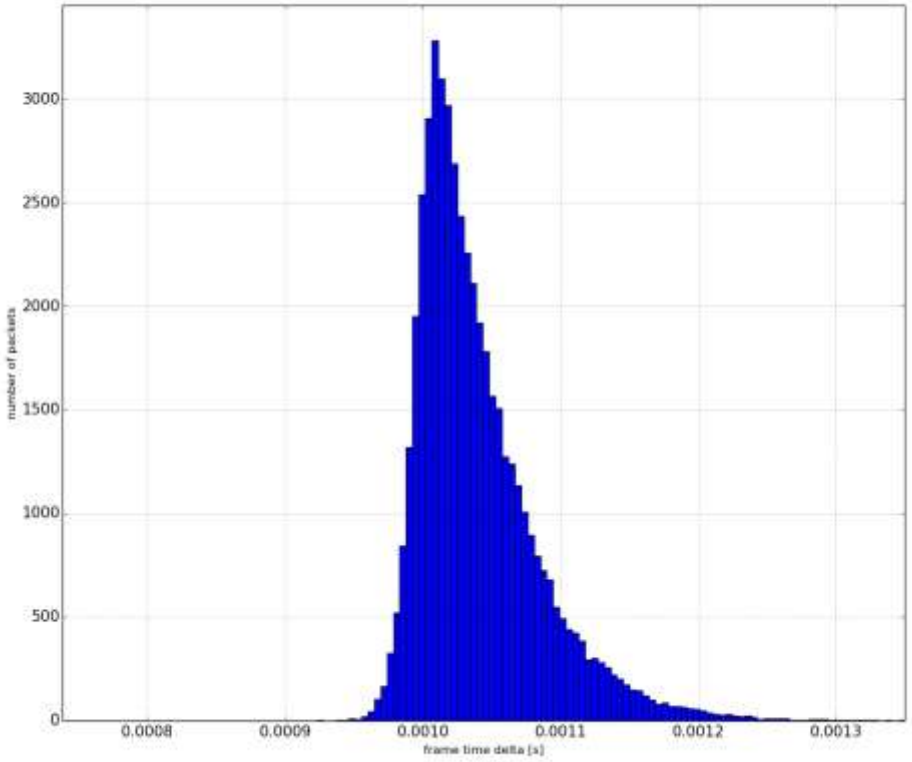
PROFINET RT on a uC?
Ramifications Issues Nr 2 & 3

- Nr 3: Too much focus on RT optimisation
  - Most PROFINET offerings don't offer good NRT traffic capabilities



PROFINET RT on a uC?
Ramifications Issues Nr 2 & 3

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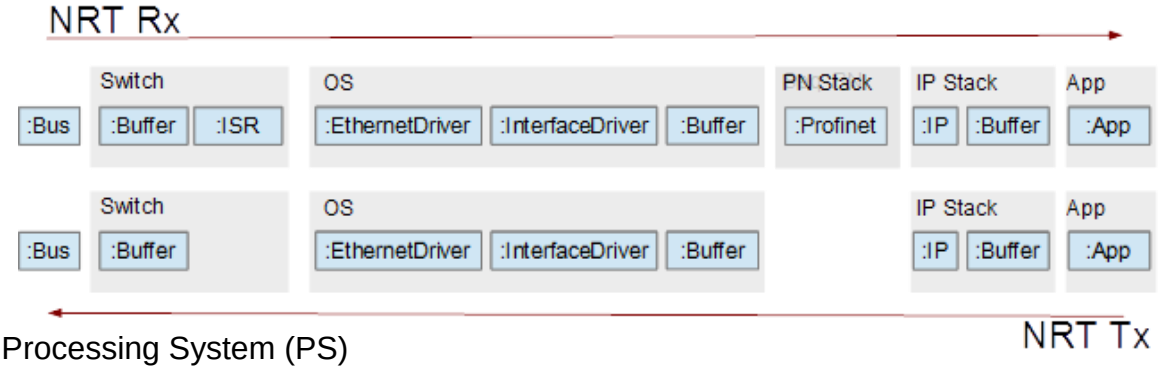
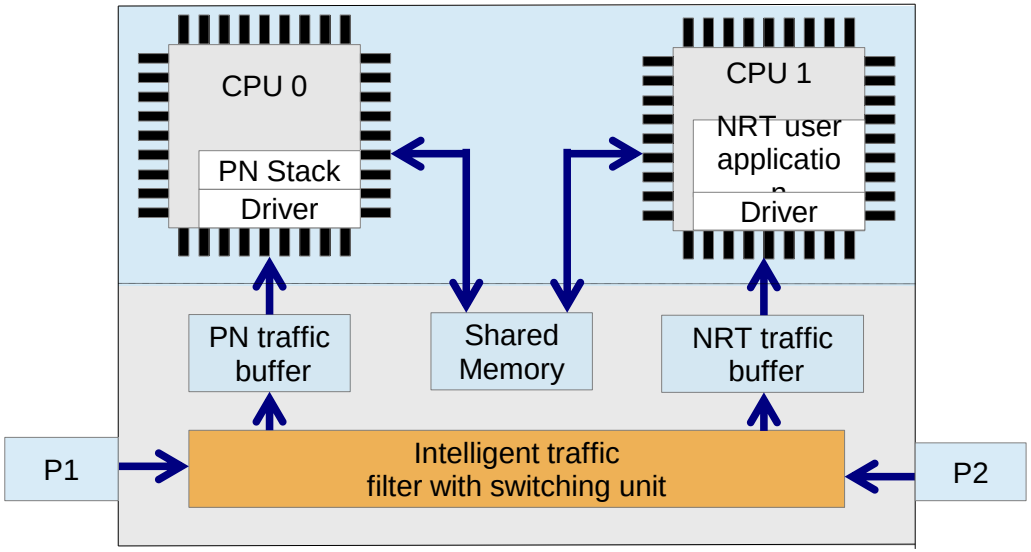
- Nr 3: Too much focus on RT optimisation
  - Problem is that RT handling has priority



Zynq Processing System (PS)



Motivated a shift towards IP solutions

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PROFINET RT on a uC?
Ramifications Issues Nr 2 & 3

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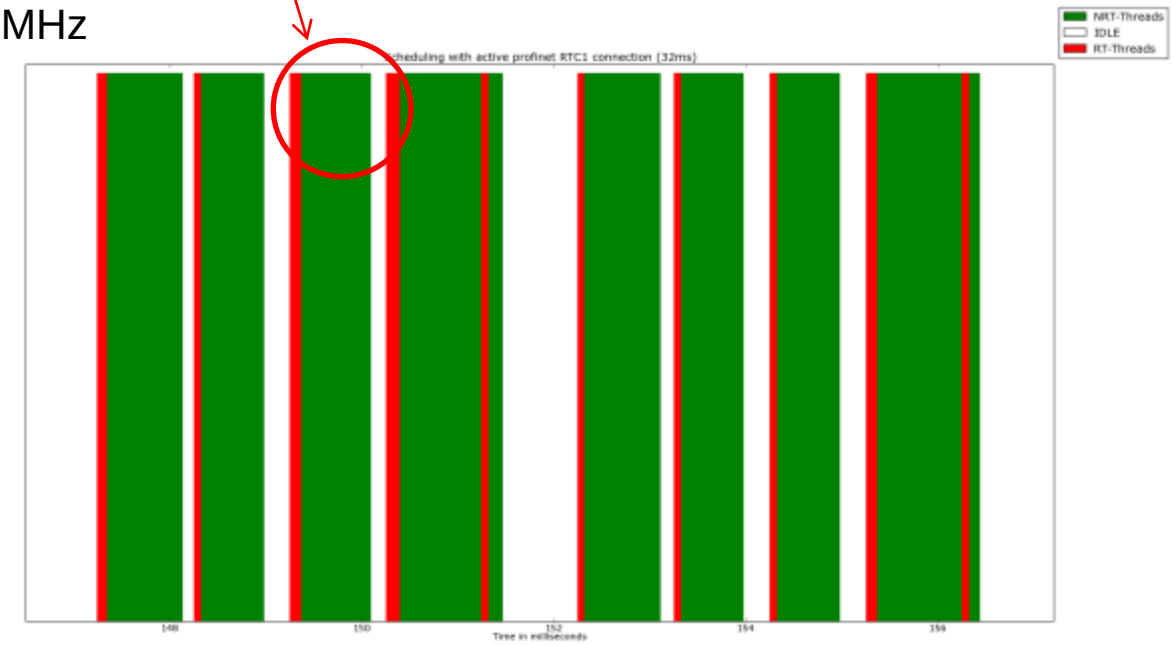
- Nr 4: Too much focus on performance RT -> What about PROFINET PA
  - Reduce the SW load for NRT
  - Cycle times > 16 ms
  - Processors < 50 MHz



PROFINET RT on a uC?
Issue Nr 4

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- Operating System and 3rd Party Software
  - PROFINET needs – RPC / UDP / IP
  - Class B/C requires SNMP (UDP / IP and sockets)
  - eCOS / Linux
    - Quality of port to platform always an issue
  - Stacks
    - f.i. Molex has ist own scheduler, RPC / UDP / IP but not SNMP
      - Either use an OS with associated IP stack or build your own system

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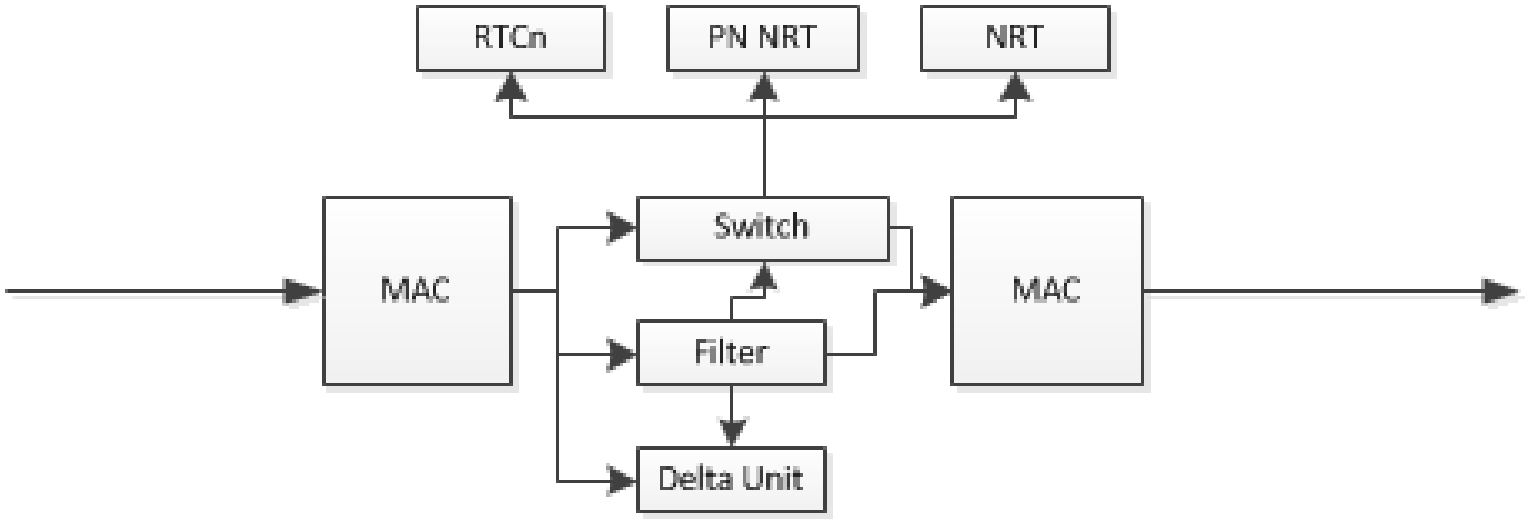
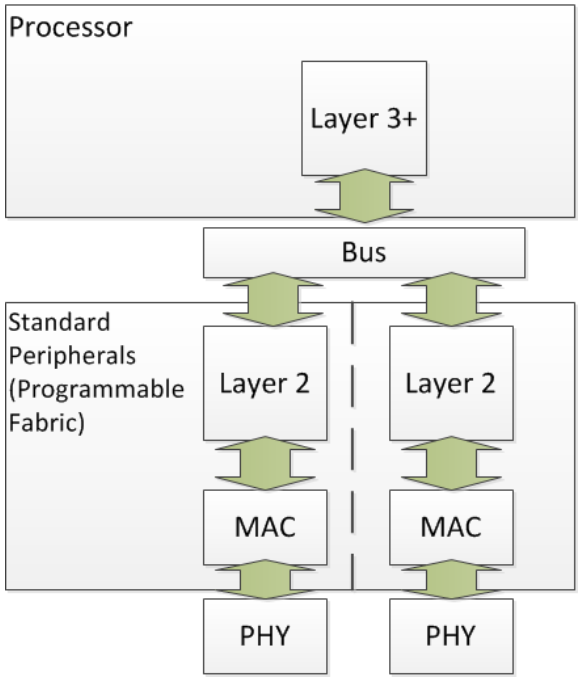
PROFINET RT on a uC?
Issue Nr 5

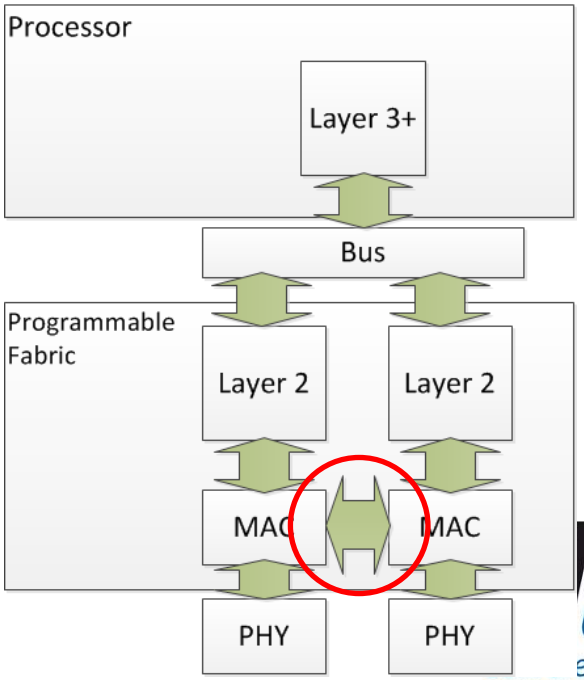
- Netload
  - Standard architectures smothered by interrupts
    - Need an appropriate buffer system
  - Faults in 3rd party SW
  - Excarbarated by connection-happy technicians



PROFINET RT on a uC?
Issue Nr 6

- Line Topologies
  - Industrial Switches are Expensive
    - Long line topologies and store-and-forward switches cause system timeouts
    - Need cut-through switching of ca. 2-3 us
    - Architecture needs to be considered





PROFINET IRT

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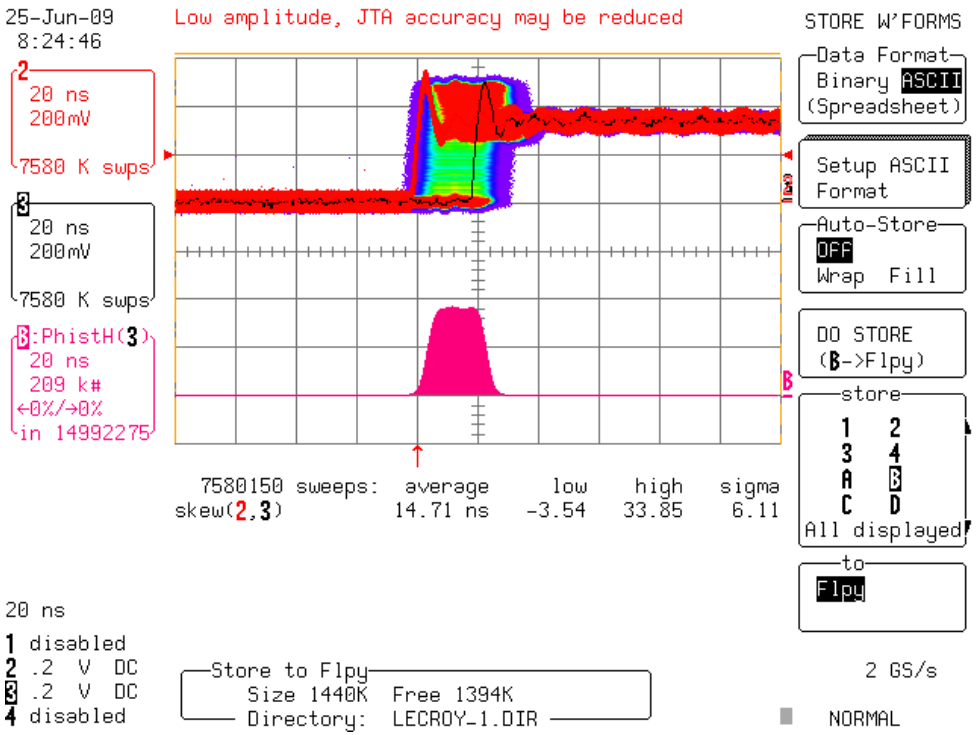
- ASIC or IP Necessary due to customised Layer 2
- All the previously discussed issues also apply
- Application and communication are synchronised using PTCP



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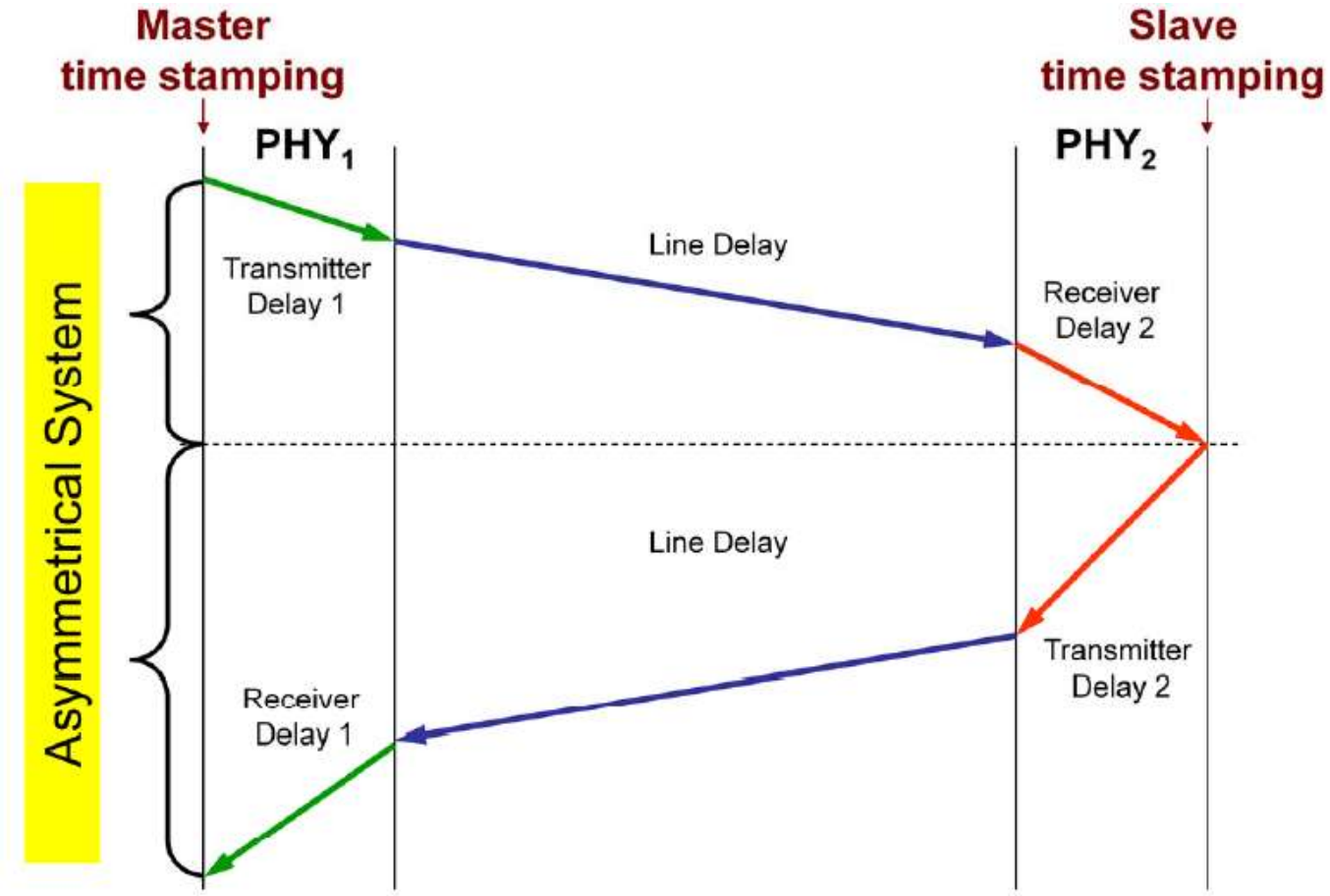
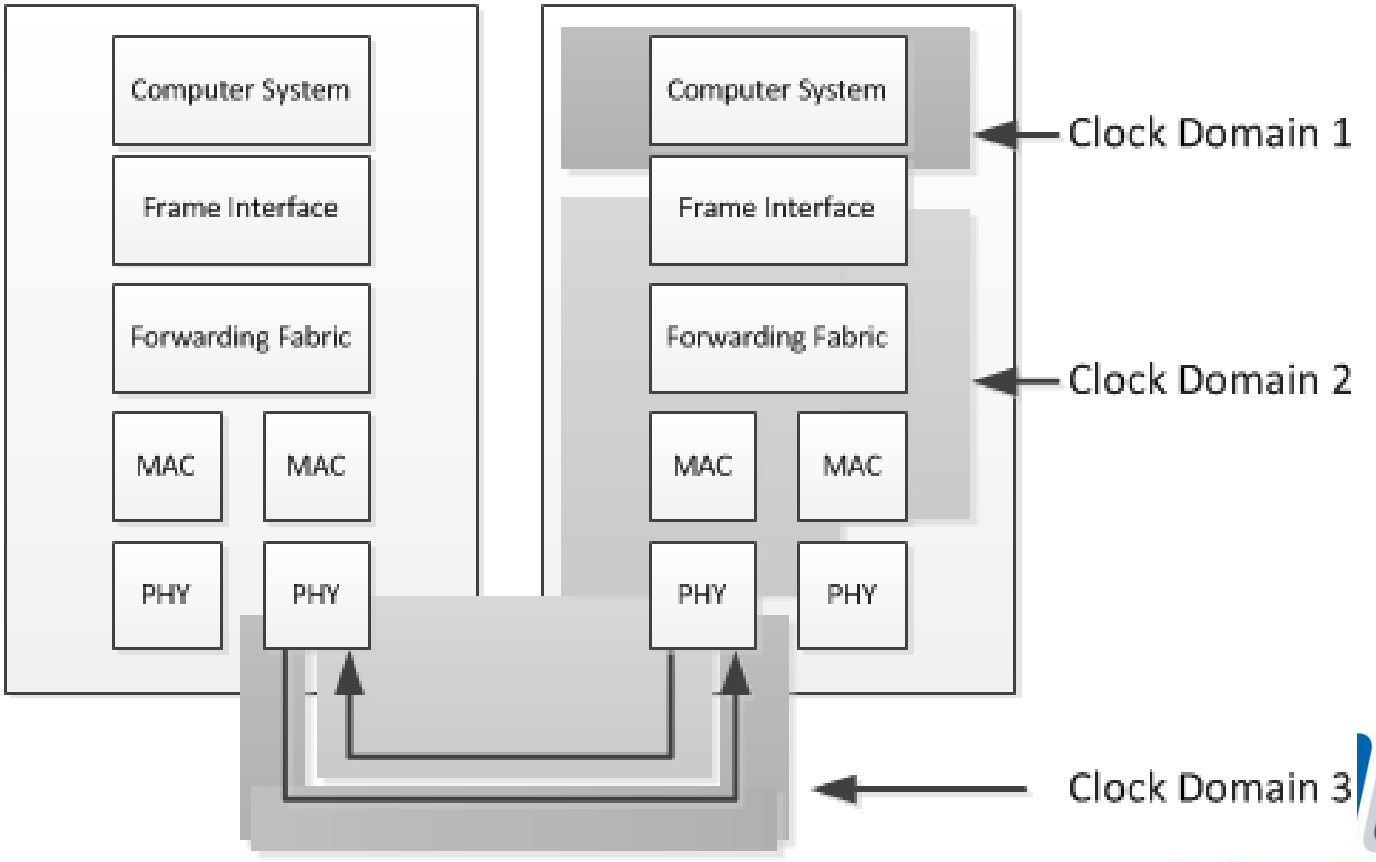
PROFINET IRT

- Tight synchronisation comes at a price – the PHY
  - Rx delay == constant + (n*8), n = [1..4]



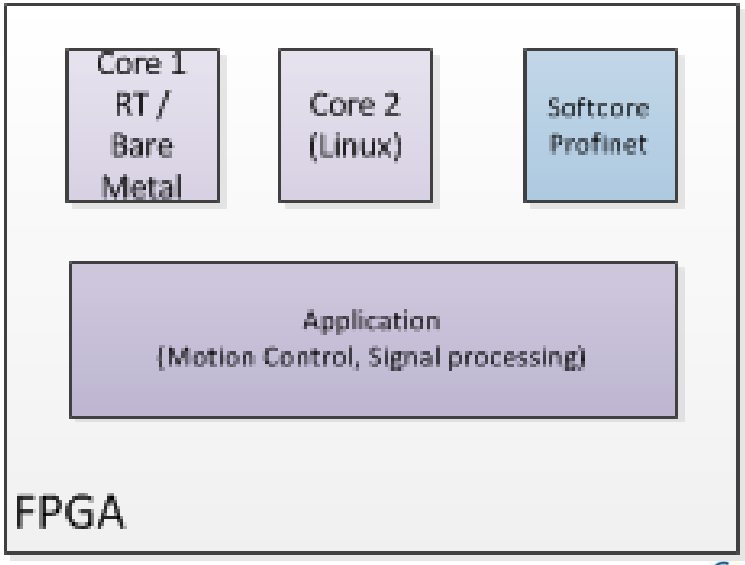
PROFINET IRT

- Tight synchronisation comes at a price – clock domains
  - Clocking Tx with the same clock as the switch doesn't hurt either



PROFINET IRT

- Sense that the communication industry is changing
  - No longer always feasible to buy a finished solution
  - Raises the question as to how much comms know-how is required to produce a reliable application
  - Re-evaluation of application architecture
  - Small shift towards FPGA solutions because its possible to offload application into FPGA



Conclusion

- PROFINET RT and IRT
  - Business case for piece rates < 1000
  - Business case 1 for ASIC's / Programmable Fabric (microcode | | FPGA)
    - Devices with small applications
  - Business case 2 for ASIC's / Programmable Fabric
    - Devices with enough real-estate and insensitive to additional chip costs
  - Business case 1 for FPGA
    - Devices where hardware offloading can increase application performance
  - Business case 2 for FPGA
    - Devices where design-in NRE costs can be recouped over a period of 2-4 years
  - Business case 3 for FPGA
    - Devices where high NRT bandwidth required

.Questions?

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Your questions are so good !

I don‘t want to spoil them with my answers.

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